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Defects and Impurities in 4H- and 6H-SiC Homoepitaxial Layers: Identification, Origin, Effect on Properties of Ohmic Contacts and Insulating Layers and Reduction

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A dry *ex situ* cleaning sequence, superior to conventional wet chemical processing, and based on UV/O_3 oxidation and exposure to the vapor of a 10:1 buffered HF solution for removal of non-carbidic C and silicon oxide, respectively, has been demonstrated via XPS analysis for $(0001)_{Si}$ 6H-SiC surfaces. Exposure to UV/O_3 resulted in a broad Si-O Si 2p peak at 102.4 eV and a shift in the non-carbidic C1s peak from 283.6 to 284.2 eV. The carbidic/non-carbidic C ratio increased from 0.8 to 2.7 after the UV/O_3 treatment. Complete removal of the silicon oxide was demonstrated via the absence of the Si-O Si 2p peak at 102.4 eV. However, significant F was detected. A chemical vapor deposition system which incorporates a separate load lock from which growth and RHEED chambers are attached has been assembled for the growth of 4H- and 6H- SiC films. Numerous safety concerns and associated placement of the system are being resolved. As-deposited NiAl, Au, Ni, and Pt contacts were rectifying on p-type 6H-SiC with very low leakage current densities (~1×10^{-8} A/cm^2 at 10 V) and displayed a similar Schottky barrier trend as previously found for n-type 6H-SiC. Ni/NiAl contacts on p-type (1×10^{19} cm^{-3}) SiC were ohmic after annealing for 10-80 s at 1000 °C with a calculated specific contact resistivity of $2\text{-}3\times10^{-2}$ W cm^2. A three-step process and associated deposition system are being developed for oxide growth on 6H- and 4H-Si. The three stages of oxide formation, namely, (1) surface preparation, (2) initial insulator formation, and (3) oxide deposition will be integrated with *in vacuo* diagnostic capabilities to facilitate an understanding of the growth process and interface electrical characteristics. High voltage Schottky barrier diodes have been successfully fabricated for the first time on p-type 4H-SiC and 6H-SiC using Ti as the barrier metal. Good rectification was confirmed at temperatures as high as 250°C. The room temperature barrier heights were $1.8_{s,sp}$) for 4H- and 6H-SiC were 25 mW cm^{-2} and 70 mW cm^{-2} at room temperature. A monotonic decrease in resistance occurs with increasing T for both polytypes due to increased ionization of dopants. An analytical model is presented to explain the decrease of $R_{s,sp}$ with T for both 4H and 6H-SiC which fits the experimental data. The critical electric field strength for breakdown was extracted in both p-type 4H and 6H-SiC using the breakdown voltage and was 2.9×10^6 V/cm and 3.3×10^6 V/cm, respectively. The breakdown voltage remained fairly constant with T for 4H-SiC; it decreased with T for 6H-SiC.

14. SUBJECT TERMS
4H-SiC, 6H-SiC, surface preparation, cleaning, UV/O_3, oxidation, carbidic C, XPS, fluorine, chemical vapor deposition, ohmic contacts, AlN, insulators, silicon oxide, deposition, Schottky barrier diode, Ti, barrier height, series resistance, electric field strength, breakdown

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I. Introduction

The two most important materials-related problems affecting the performance of all SiC devices and their associated components (e.g., contacts) are the defects and the undesired impurities which become incorporated in the homoepitaxial SiC layers in which all devices are currently fabricated. Bhatnagar [1] has shown that the reverse blocking leakage current in high voltage Schottky diodes is three orders of magnitude higher than theoretically predicted as a result of defects in the epi-layer. The formation of micropipes, stepped screw dislocations, interacting dislocation loops, polyganized networks of dislocations and growth twins as well as stacking faults during the sublimation growth of SiC boules are likely the root cause of some of the defects in the epitaxial layer. However, with the exception of the micropipes, the types and concentrations of line, planar and other three-dimensional defects and their effect on the performance of devices and individual device components in the important epi-layer have not been similarly determined. As such, it is not known which of the latter defects actually are translated from the wafer into the epi-layer during its deposition and, therefore, should be vigorously controlled during boule growth and which defects are generated during deposition.

The relatively uncontrolled occurrence of the n-type donor of N and deep level compensating impurities such as Ti in the epilayer have been identified via secondary ion mass spectrometry, photoluminescence and cathodoluminescence investigations. However, the origins of essentially all of these impurities are unknown. For high-temperature, -power and -frequency devices, it is highly desirable to control or eliminate these impurities such as to attain undoped films with uncompensated carrier concentrations of 10^{14} cm^{-3}—two orders of magnitude lower than what is, at present, normally achieved in standard commercial depositions.

The formation of low resistivity and thermally stable ohmic contacts to 4H- and 6H-SiC remains a serious problem in the development of SiC device technology. For SiC power devices to have an advantage over Si, the contact resistivities must be below 1×10^{-5} W-cm^2, as noted by Alok, *et al.* [2]. In addition, the electrical characterization of state-of-the-art SiC films depends on the ability to fabricate ohmic contacts on material with low carrier concentrations. Therefore, better ohmic contacts are needed both for improving device performance and for improving the quality of films which can be grown. The thermal stability of ohmic contacts is of particular concern for p-type SiC, which have traditionally relied on low melting point Al or Al alloys to dope the SiC surface below the contacts. These materials are not suitable for devices intended for high-temperature operation. While the fabrication of ohmic contacts to SiC has also normally depended on the attainment of a very heavily-doped near-surface region, the introduction during deposition of high levels of dopants in the near surface device region of the epi-layer prior to the deposition of the contact or by ion implantation through the contact makes probable the introduction of point and line defects as a result of the induced strain in the lattice.

Based on all of these issues and recent experiments already performed at NCSU, our goals are to produce contacts which are thermally stable and have low contact resistivities while also reducing the need for doping by ion implantation.

To fabricate most microelectronic devices, the growth or deposition of stable insulators is needed to provide both passivating layers and gate dielectrics. Silicon carbide is almost invariably thermally oxidized, albeit at a slower rate, in the same manner and temperature range that is employed for Si. Most of the previous studies regarding the oxidation of SiC have been concerned with polycrystalline materials. It has been shown by Harris and Call [3] and Suzuki, *et al.* [4] that the (0001) face of 6H-SiC oxidizes according to the same linear-parabolic equation reported for Si by Deal and Grove [5]. The model states that the initial stage of oxidation is reaction rate limited and linear, but becomes parabolic as the diffusion of the oxidant through the oxide becomes the rate limiting factor. Research at NCSU by Palmour, *et al.* [6] has demonstrated that the oxidation process on SiC in wet and dry oxygen and wet argon obeys the linear-parabolic law. Both wet processes had a slower rate than dry oxidation at 1050°C and below. The dry oxides exhibited a very flat surface; in contrast, SEM and TEM revealed that wet oxidation preferentially oxidizes dislocation bands, causing raised lines on the oxide and corresponding grooves in the SiC. It was proposed that the much higher solubility of H_2O in SiO_2 as compared to that of O_2 allows wet oxidation to be preferential.

All of the oxidation studies on all polytypes of semiconductor quality SiC have been conducted on n-type material with the exception of the investigation by Palmour *et al.* [6]. The objective of this study was the determination of the redistribution of the common electrical dopants of N, P, Al and B during thermal oxidation of SiC films at 1200°C in dry O_2. Experimental segregation coefficients and interfacial concentration ratios were determined. Secondary ion mass spectrometry revealed that B and Al depleted from the SiC into the growing oxide while N and P were found to pile up in the SiC as a result of the loss of the SiC to the oxide formation. Aluminum is now used almost universally as the p-type dopant in SiC. The electrical properties of oxides thermally grown on n-type SiC normally have reasonably favorable characteristics of high breakdown voltage and low leakage currents. However, the reverse is true for thermally grown oxides on p-type SiC, as shown by Baliga and his students at NCSU. It is believed that at least two of the causes of the poor performance on a p-type material are the existence of the Al in the oxide and at the oxide/SiC interface and the dangling oxygen bonds which this species creates in the oxide as a result of a difference in oxidation state (+3) compared to that of Si (+4) and the existence of C at the SiC/insulator interface. Methods of effectively cleaning SiC surfaces prior to oxidation to deposit and grow oxides on p-type material under UHV conditions and determine the effect of Al redistribution and C concentrations at the interface on the properties of the oxide must be determined. In addition,

the effect of existing line and planar defects in the SiC epi-layer on the properties of the thermally grown and deposited oxide must be ascertained.

The research conducted in this reporting period and described in the following sections has been concerned with (1) the determination and employment of an effective, completely dry, *ex situ* hydrocarbon and oxide removal process for the 6H-SiC(0001) surface, (2) design and construction of a new CVD SiC system for the deposition and doping of 6H- and 4H-SiC and AlN films, (3) deposition, annealing and electrical characterization of Ni, NiAl, Au, Pt and Cr-B contacts to p-type SiC(0001), and (4) fabrication for the first time of high voltage Schottky barrier diodes on 4H- and 6H-SiC(0001) and determination of the associated barrier heights, series resistance and critical electric field strength for breakdown as a function of T. The following individual sections detail the procedures, results, discussions of these results, conclusions and plans for future research. Each subsection is self-contained with its own figures, tables and references.

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II. Dry *Ex Situ* Cleaning Processes for $(0001)_{Si}$ 6H-SiC Surfaces

A. Introduction

For SiC to succeed as the semiconductor/substrate of choice for high frequency/high temperature, high power devices and III-N heteroepitaxy, a considerable reduction in defects (line, planar, point, etc.) must be achieved. Following Si technology, where surface cleaning and preparation are critical first steps in all processes [1], a continued reduction in defects in SiC should be expected as a result of improved SiC wafer surface cleaning techniques. In Si technology for example, improper removal of surface contamination and oxides prior to Si homoepitaxy has been shown to result in an increase in the density of line and planar defects in epitaxial films from $< 10^4/cm^2$ to $> 10^{10}/cm^2$ [2-4]. These increased defect densities were in turn found to correspond with a decrease in device yield [5]. In the case of heteroepitaxy, studies on Si_xGe_{1-x} alloy growth on Si (100) have additionally shown that surface defects produced in the Si substrate by residual organic/carbon contamination act as the preferred sites for misfit dislocation generation [6]. These examples clearly illustrate that surface preparation and cleaning should be equally important to the control of defects in both homoepitaxial and heteroepitaxial growth of SiC and III-V nitrides on (0001) 6H-SiC.

Due to a limited number of studies concerned with *ex situ* SiC cleaning practices [7-10], most SiC *ex situ* wet chemical processing has been based on processes specifically developed for and employed in Si technology [10,11]. Silicon carbide *ex situ* cleaning/surface preparation has typically consisted of some variation of solvent degreasing, organic contaminant removal using RCA or Piranha cleans, and finishing with oxide removal using an HF based solution [7-11]. However, an important assumption underlying the use of these procedures is that SiC surfaces should behave similar to silicon surfaces in these wet chemicals. In fact in a previous paper, examples were provided of where this assumption fails specifically with regard to oxide removal from SiC with an HF dip. In Si technology, oxide removal with HF is known to generate a hydrophobic, hydrogen terminated surface, stable against oxidation in air for several hours [12-17]. However, it has previously been shown that SiC surfaces are inherently hydrophilic after oxide removal with HF [18]. The hydrophilic surface allows water and HF to become trapped in mircopipes in the SiC wafer which can lead to large concentrations of oxygen and fluorine at the SiC/dielectric interface if not properly outgassed. In order to produce a hydrophobic surface, passivation/capping layers based on silicon and/or fluorocarbons were required [18].

An alternative to the use of passivation layers to form hydrophobic SiC surfaces would be to develop a completely dry *ex situ* cleaning process and, thus, remove the need for a hydrophobic surface. In Si and GaAs technology, dry removal of carbon contaminants from surfaces using UV/O_3 oxidation has become a popular alternative to wet chemical

processing [19-25]. In UV/O_3 oxidation, UV radiation from a Hg lamp (specifically the 184.9 nm line) is used to photo excite molecular oxygen (O_2) to generate ozone (O_3). The 253.7 nm line of Hg is in turn adsorbed by O_3 to form atomic O. Atomic oxygen and ozone are extremely reactive species which rapidly oxidize organic contaminants forming CO and CO_2 which desorb from the surfaces. The 253.7 nm line of Hg also assists in removal of carbon contaminants as it is adsorbed by most hydrocarbons and excites C-H and C-C bonds. Removal of the UV/O_3 generated surface oxides is typically achieved by wet chemical processing and/or *in situ* thermal desorption [19,20,22,24]. However, Iyer *et al.* [25] have shown that the equilibrium vapor from an HF solution can be alternatively used to remove the native oxide from a silicon wafer via a dry *ex situ* process. Thus, the combined use of UV/O_3 oxidation for removal of carbon contaminants and HF vapor exposure for oxide removal represents a completely dry *ex situ* cleaning process. Completely dry *ex situ* cleaning processes are advantageous not only for working with hydrophilic surfaces but are economical and environmentally friendly. Use of completely dry processing techniques eliminates the need for large quantities of expensive high-purity chemicals while simultaneously reducing the costs for disposal of these toxic materials [26-28]. The use of smaller quantities of wet chemicals also has the added benefit of minimizing the amount of toxic chemicals released into the ecosystem [26].

In this paper, we demonstrate for the first time a completely dry *ex situ* cleaning process for $(0001)_{Si}$ 6H-SiC surfaces which is based on the combined use of UV/O_3 oxidation and HF vapor cleaning. This clean has been found to be equivalent to or better than typical wet chemical processes in terms non-carbidic carbon and oxide contamination levels as measured by XPS. The combined UV/O_3-HF vapor treatment eliminates the need for a hydrophobic SiC surface and avoids the use of exotic passivation layers.

B. Experimental Procedure

On axis, n-type (typically $N_d=10^{18}/cm^3$) $(0001)_{Si}$ 6H-SiC wafers were used in these experiments. Prior to UV/O_3 oxidation, each wafer was first ultrasonically degreased in trichloroethylene, acetone, and methanol for 10 min. each. The UV/O_3 treatments described in this study employed a box in which a high intensity Hg lamp was positioned in close proximity ($\approx$ 1 cm) to the SiC wafer (see Fig. 1). In order to increase the concentration of O_3 generated (i.e. to increase oxidation rate), the UV/O_3 box was purged with 1 L/sec O_2 during the UV exposure. Further details of this process have been described previously [20]. HF vapor cleans were achieved by simply positioning the SiC wafer within approximately 5 mm of a 10:1 buffered HF solution for times ranging from 5-30 min. (see Fig. 1). Condensation of HF on the SiC surface was not observed for exposures of this length.

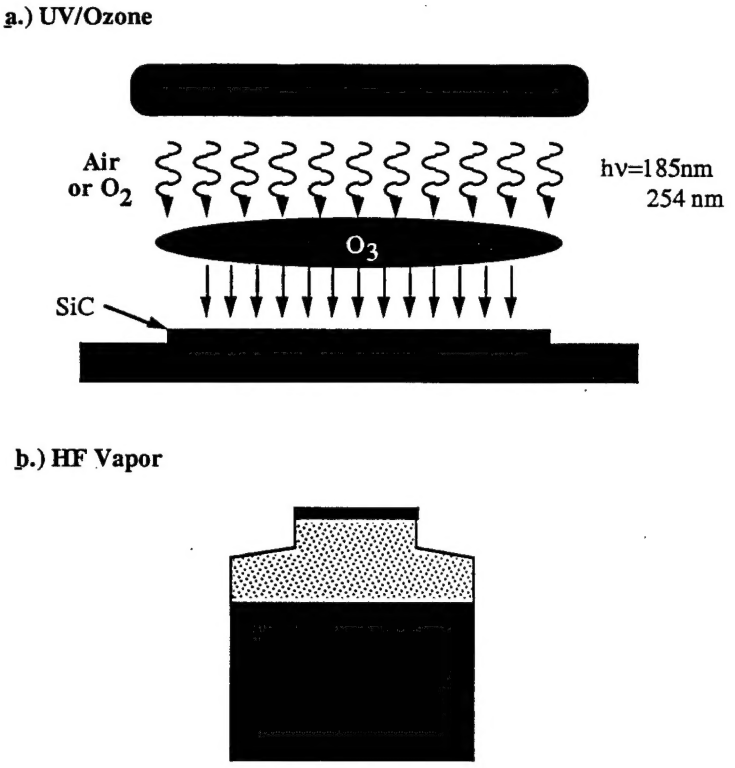

Figure 1. (a) Schematic of UV/O_3 oxidation system and (b) schematic of HF vapor procedure.

Surfaces prepared in the above manner were subjected to surface analysis in an integrated ultra-high vacuum system incorporating the following analytical techniques: X-ray Photoelectron Spectroscopy (XPS), Auger Electron Spectroscopy (AES), Electron Energy Loss Spectroscopy (EELS), and Low Energy Electron Diffraction (LEED). Details of this system are given elsewhere [29]. After each treatment above, the SiC wafer was mounted to a molybdenum sample holder and loaded into a load lock for subsequent analysis by AES, XPS, EELS, and LEED. XPS analysis was performed using the Al anode (hν=1486.6 eV) at 20mA and 12 kV. AES spectra were obtained using a beam voltage of 3 keV and an emission current of 1 mA. EELS spectra were obtained using a 100 eV electron beam and an emission current of 1 mA. LEED was performed using rear view optics, a beam voltage of approximately 115 eV, and an emission current of 1 mA. Calibration of the XPS binding energy scale was performed by measuring the position of the Au $4f_{7/2}$ and shifting the spectra such that the peak position occurred at 83.98 eV.

C. Results

Solvents and UV/O_3. Figures 2(a) and (b) show XPS spectrums of the C 1s core level taken from a $(0001)_{Si}$ 6H-SiC surface before and after a UV/O_3 oxidation treatment. As can be seen in Fig. 2(a), a fairly broad C 1s spectrum was observed prior to UV/O_3 oxidation. Data analysis of this spectrum revealed the presence of two C 1s peaks centered at 282.5 and

283.6 eV which were assigned to carbidic (C-Si) and non-carbidic (C-C, C-H, etc.) carbon, respectively. The large FWHM (full width half maximum) of 2.6 eV for the non-carbidic C1s peak suggests that the non-carbidic carbon is a mixture of C-C and C-H bonding states. In addition, we have previously detected from these surface traces of non-carbidic carbon centered at 286.0 eV which may be indicative of C-F bonding [18]. Following a two-hour UV/O_3 treatment, a large shift in the non-carbidic C1s peak from 283.6 to 284.2 eV was observed. This was in contrast with the carbidic C1s peak which only increased by 0.1 eV to 282.6 eV. In addition, the carbidic/non-carbidic carbon ratio was observed to increase from 0.8 to 2.7 after the UV/O_3 treatment. The shift and reduction in the non-carbidic C1s peak is consistent with the formation of C-O bonding at the surface and removal of some non-carbidic carbon via desorption of CO and CO_2.

XPS of the Si 2p core level from the $(0001)_{Si}$ 6H-SiC surface before and after UV/O_3 treatment (see Figs. 3a and 3b) additionally shows the formation of silicon oxides on the surface. As shown in Fig. 3a, a single Si 2p peak is detected before UV/O_3 oxidation. The line shape of this Si 2p peak is asymmetric suggesting the possibility of a Si-O bonding peak on the higher BE (binding energy) side. Unfortunately, deconvolution of this peak is complicated by the fact that the Si 2p peak is really an unresolved doublet (i.e. Si $2p_{3/2,1/2}$). As such, it was not possible to irrefutably determine whether a Si-O peak existed. However, after the UV/O_3 treatment, a broad Si-O peak centered at 102.4 eV (FWHM=2.1 eV) was clearly detected (see Fig. 3b). The width of the Si 2p peak at 102.4 eV indicates that silicon in +2,+3, and +4 oxidation states is bonded to the oxygen (i.e. Si-O, O-Si-O, Si=O).

In a previous paper, it was demonstrated that the surfaces of as received on and off axis $(0001)_{Si}$ 6H-SiC wafers were covered with a thin layer of fluorocarbon contamination [18]. As such removal of this contamination layer by UV/O_3 oxidation should be evidenced by a reduction in the F 1s peak which is exactly what was observed. As shown in Figure 4(b), two F 1s peaks at 685.4 and 687.2 eV were detected from the $(0001)_{Si}$ surface prior to oxidation. These two peaks were assigned to Si-F and C-F bonding respectively. After the UV/O_3 treatment, only a slight trace of the lower binding energy F 1s peak was detected and it was observed to shift by 0.5 eV to 685.9 eV (see Fig. 4c). The higher binding energy peak at 687.2 eV believed to be due to fluorine bonded to carbon was completely eliminated indicating removal of any fluorocarbons present on the surface.

HF Vapor. After oxidation of the $(0001)_{Si}$ 6H-SiC surface using a UV/O_3 treatment, removal of the thin silicon oxide layer grown on the surface was achieved by exposing the SiC surface to the vapor from a 10:1 buffered HF solution for 30 min. As shown in Fig. 3(c), the higher binding energy Si 2p peak centered at 102.4 eV was completely removed by the HF vapor treatment. Shorter HF vapor treatments were observed to still leave a Si-O Si2p peak at much larger BE ($\approx$104 eV).

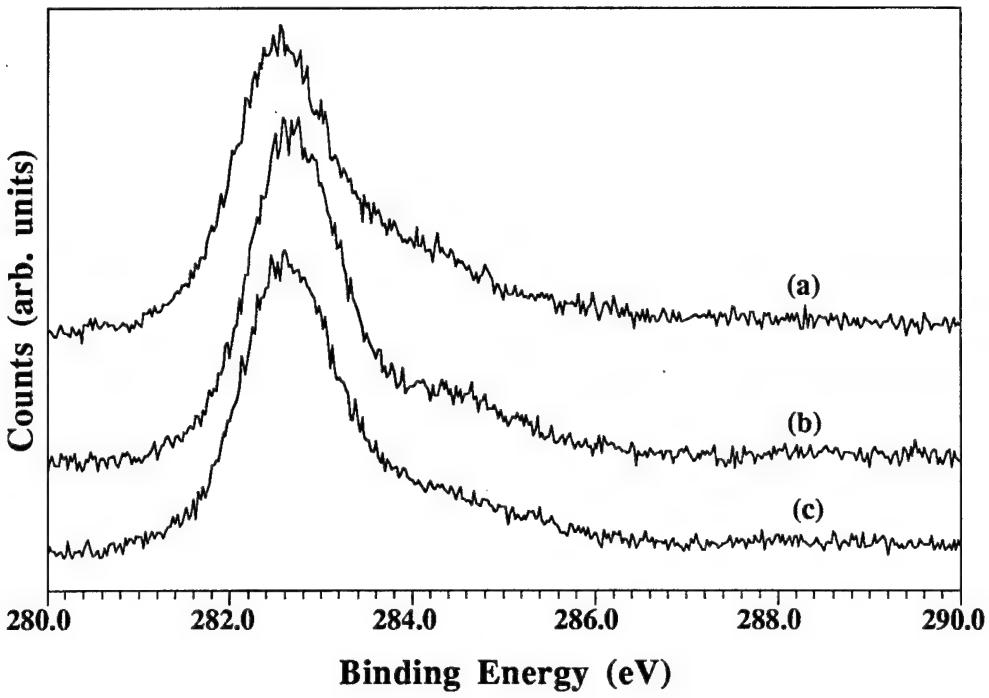

Figure 2. XPS of C 1s from on axis $(0001)_{Si}$ 6H-SiC after (a) solvent cleaning, (b) UV/O_3, and (c) HF vapor cleaning.

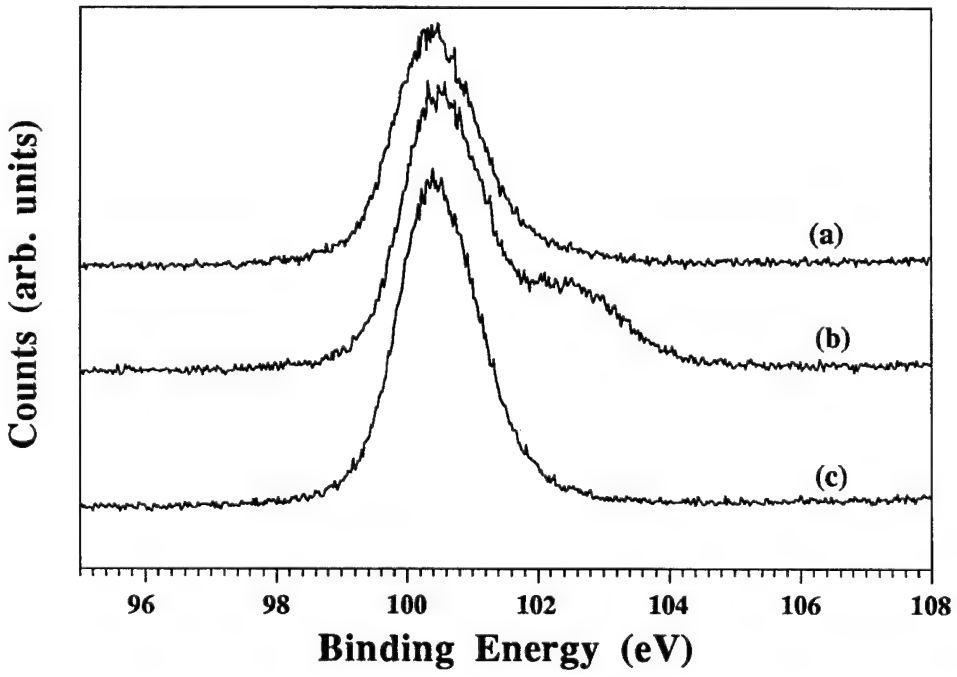

Figure 3. XPS of Si 2p from on axis $(0001)_{Si}$ 6H-SiC after (a) solvent cleaning, (b) UV/O_3, and (c) HF vapor cleaning.

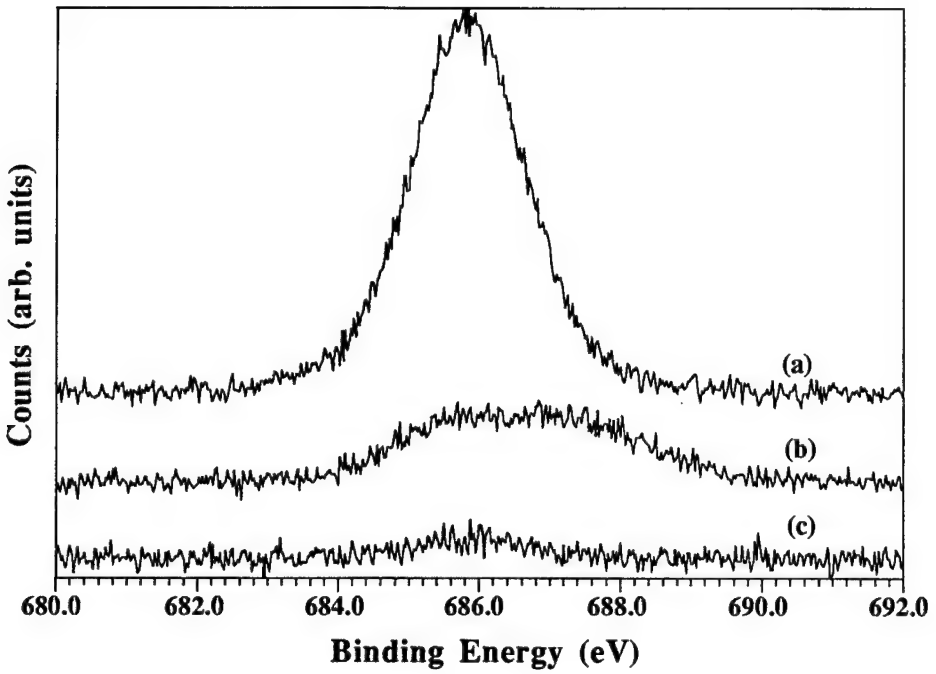

Figure 4. XPS of F 1s from on axis $(0001)_{Si}$ 6H-SiC after (a) HF vapor cleaning, (b) solvent cleaning, and (c) UV/O_3.

Table I. Core Levels Positions from $(0001)_{Si}$ 6H-SiC after Various Treatments

	Si 2p (FWHM)	C 1s	O 1s	F 1s
Solvents	100.4, 1.5	282.5, 1.1 283.6, 2.6	531.6, 2.3	685.4, 1.8 687.2, 2.7
UV/O_3	100.5, 1.4	282.6, 1.1 102.4, 2.1	532.1, 2.4 284.2, 2.1	685.9, 1.9
HF Vapor	100.5, 1.5	282.6, 1.1 283.8, 2.8	531.8, 2.3	685.8, 1.9

Table II. Core Level Ratios from $(0001)_{Si}$ 6H-SiC after Various Treatments

	carbidic/noncarbidic	Si/O	Si/F
Solvents	0.8	1.1	5.4
UV/O_3	2.7	0.3	10.6
HF Vapor	1.7	1.3	0.5

After the HF vapor treatment, the amount of non-carbidic surface carbon was observed to increase with the corresponding carbidic/non-carbidic carbon ratio decreasing from 2.7 to 1.7. The non-carbidic C1s peak was likewise observed to shift down to 283.8 eV and with a huge increase in FWHM from 2.1 to 2.8 eV. However, the carbidic/non-carbidic carbon ratio of 1.7 after the HF vapor treatment is still much larger than the 0.8 that was found after only solvent cleaning.

In addition to an increase in non-carbidic carbon after the HF vapor treatment, the amount of fluorine on the surface was also observed to increase dramatically (see Fig. 4a). Prior to the HF vapor treatment, the Si/F ratio was equal to 10.6. However, after the HF vapor treatment the Si/F ratio plummeted to 0.56. Further, the position of the F 1s was not observed to shift but remained centered at 685.9 eV which suggests that fluorine is bonded only to silicon atoms at the surface.

D. Discussion

UV/O_3 Oxidation. In the above section, it was demonstrated that exposure of $(0001)_{Si}$ 6H-SiC surfaces to ozone generated by a Hg UV lamp oxidized and removed non-carbidic carbon from the SiC surface. This resulted in an increase of the carbidic/non-carbidic carbon ratio from 0.8 to 2.7. This result is in agreement with previous studies of UV/O_3 oxidation of Si and GaAs surfaces which have also shown a removal of carbon contaminants [19-24]. However, some non-carbidic carbon was observed to be still present on the SiC surface after the long UV/O_3 treatment. Some of this non-carbidic carbon is surely due to recontamination of the SiC surface during sample transfer and mounting in a laboratory ambient prior to insertion into vacuum. However, contamination levels of this magnitude are usually not observed from silicon wafers cleaned in the same environment. Alternatively, the remaining non-carbidic carbon could be due to carbon trapped in the silicon oxide layer and or carbon bonded to both silicon and oxygen at the SiC/silicon oxide interface. The shift in the position of the non-carbidic C 1s peak from 283.6 to 284.2 eV with UV/O_3 oxidation is in the direction expected for oxidation of carbon. For HF dipped Si wafers, it has been previously determined that residual carbon contaminants with C 1s peaks positions of 284.6, 286.3, and 288.4 eV are composed mostly of $C\text{-}H_2$, C-O, and O-C=O bonded carbon respectively [30]. Additionally, the C 1s peak position from graphite is known to occur at 284.5 eV [31]. Unfortunately, a direct comparison between the non-carbidic C1s peak position/bonding configuration for both Si and SiC surfaces is complicated by the probable existence of 0.5-1.0 eV of band bending at the SiC surface due to surface Fermi level pinning. Pinning of the Fermi level causes the binding energy of the C 1s (and Si 2p, O1s, etc.) peak positions to be decreased by 0.5-1.0 eV relative to their corresponding "bulk" values. However, as HF dipped Si surfaces are known to exhibit a flat band condition, one can a priori add 1.0 eV to the SiC C1s core levels and see that

prior to UV/O_3 the non-carbidic carbon is composed of mostly C-C and CH_2 bonds and after the UV/O_3 treatment the non-carbidic carbon is closer to C-O bonding. The authors also note that the studies of Fominski *et al.* [32] and Baunack and Zehe [24] do not report complete removal of carbon contaminants from Si surfaces using O_3 generated from a Hg lamp. In fact, Fominski *et al.* [32] found it necessary to switch to deeper UV from a D_2 lamp and use an $O_2/NF_3/H_2$ gas mixture. Complete removal of non-carbidic carbon via UV/O_3 oxidation to the authors knowledge has only been clearly demonstrated for GaAs surfaces and even then it is debatable whether the carbon is removed or just buried at the GaAs/oxide interface.

Although the UV/O_3 oxidation treatment was not completely successful in removing all of the non-carbidic carbon from the SiC surface, a comparison of this technique with other wet chemical techniques does show the utility of the technique. In a previous paper, we examined the effect that standard wet chemical treatments such as RCA SC1 and Piranha etch have on the removal of the same carbon surface contamination observed in this study. Table III provides a direct comparison of the carbidic/non-carbidic carbon and Si/O ratios for each treatment. As can be seen, the UV/O_3 treatment provides the highest carbidic/non-carbidic ratio of all the treatments examined and is, therefore, the best at removal of carbon contaminants. The authors additionally note that UV/O_3 oxidation over RCA cleaning has been recently demonstrated by Afanas'ev *et al.* [33]. Their results have found UV/O_3 oxidation to be a useful cleaning/pre-oxidation procedure prior to thermal oxide growth for SiC/SiO_2 MOS structures. In comparison to RCA cleaned SiC samples, they observed that the UV/O_3 pre-oxidation treatment resulted in a reduction defect species (fast interface states) and positive charge at the SiC/SiO_2 interface from $2\times10^{12}/cm^2$ to $6\text{-}8\times10^{11}/cm^2$. They propose/speculate that the reduction in positive charge by the UV/O_3 treatment is due to the removal of carbon clusters (i.e. C-C bonding) left on the SiC surface after growth of epitaxial layers and which are not removed by RCA cleaning or the thermal oxidation process itself. The authors note that this speculation is supported by our observation that UV/O_3 oxidation removed and shifted non-carbidic carbon or C-C and $C\text{-}H_2$ bonding on our SiC surfaces to higher oxidation states.

Finally, the authors note the enhanced ability of the UV/O_3 to oxidize SiC surfaces in comparison to other standard wet chemical treatments such as RCA SC1, and boiling aqua regia which are known to form passivating oxides on silicon. As shown in Table III, the Si/O ratio of 0.3 produced by a UV/O_3 treatment is much lower than the $\approx$ 1.0 produced by wet chemical treatments such as boiling Aqua Regia and RCA SC1. In fact, this ratio is not significantly different from the Si/O ratio of 1.1 observed from solvent cleaned SiC surfaces. However, this observation is consistent with the known inability of any of these acids to etch SiC. Therefore, the ability of UV/O_3 to grow a thin (10-20 nm) passivating oxide is an added benefit over conventional wet chemical processing. Also, the ability to form the passivating

Table III. Summary of Carbidic/Non-carbidic Carbon and Si/O Ratios from XPS Data

Treatment	Carbidic/Non-carbidic	Si/O
Solvents	0.8	1.1
Piranha	1.1	0.9
RCA SC1	2.2	1.0
Aqua Regia	1.2	1.2
UV/O_3	2.7	0.3
HF dip	6.6	1.4
HF vapor	1.3	1.2

oxide at room temperature is an additional bonus as thermal oxidation of SiC typically requires temperatures of 1000-1200°C [34]. Lastly, the authors note that the Si 2p spectrum generated from SiC by UV/O_3 oxidation (see Fig. 3b) bares a striking resemblance to the Si 2p spectra obtained from a SiC sample exposed to a total fluence of 9×10^{21} oxygen atoms (i.e. O instead of O_2) during low earth orbit on a satellite [35]. This suggests that UV/O_3 oxidation could be used to simulate the operational conditions of SiC devices in outer space and other harsh oxidizing environments.

HF Vapor. As Figures 2(b) and 2(c) show, the equilibrium vapor from an HF solution alone can be used to effectively remove silicon oxides from SiC surfaces. Though Fig. 2(c) shows the complete removal of the higher BE Si 2p peak at 102.4 eV, some oxygen was observed to remain on the SiC surface (probably in the form of suboxides of silicon and carbon i.e. C_3-Si-O and Si_3-C-O). Table III shows that the resulting Si/O ratio after the vapor treatment was observed to increase from 0.3 to 1.3. The Si/O ratio of 1.3 compares well with the value of 1.4 obtained from a SiC surface after removal of a thermal oxide with a 10:1 HF dip [18]. This clearly illustrates that HF vapor exposure is equally as effective as HF dips in removing surface silicon oxides from SiC surfaces. The authors do note, however, that the silicon oxide etch rates for HF vapor and HF dips are extremely different. In the HF vapor case, 30 minutes is required to remove only 10-20 nm of UV/O_3, whereas in the HF dip case, only 10 minutes were required to remove 100 nm of thermal oxide.

Unfortunately, the carbidic/non-carbidic carbon ratio was observed to decrease from 2.7 to 1.7 after the HF vapor treatment. Most of this can be blamed on the laboratory environment. A much smaller decrease would be expected for HF vapor treatments conducted in a clean room environment.

The authors also note that the HF vapor treatment left a significantly large amount of fluorine on the SiC surface. The observed fluorine coverage following the HF vapor treatment was 3-4 times larger than that observed from SiC wafers dipped in 10:1 HF and blown dry

without a de-ionized water rinse. The fluorine surface coverage approaches that of 1/2-full monolayer. As the peak position of the F 1s core level after the HF vapor treatment remains essentially unchanged at 685.9 eV (i.e. Si-F bonding), this suggests that the HF vapor treatment leaves a Si-F terminated SiC surface. These results are in contrast with those of Iyer *et al.* [25] for silicon (100) in which no fluorine was detected by XPS and hydrogen termination was confirmed by TPD. These results might explain the observed partial hydrophobic nature of SiC surfaces on removal from HF solutions where partial fluorine coverage has been found, and the observed hydrophilic nature of SiC surfaces after rinsing in de-ionized water which has been found to remove/rinse fluorine from the surface [18]. Perhaps in contrast to Si, fluorine termination of SiC surfaces is favored over hydrogen termination. For silicon, it has been reasoned that hydrogen termination exist due to the fact that the energy level of the hydrogen ion in solution corresponds closely to the top of the Si valence band [26]. In contrast, 6H-SiC has a wider band gap of 3.0 eV and hence the SiC valence band maximum will lie well below that of the hydrogen ion in HF. However, the fluorine ion is more electronegative and will lie at a lower energy level much closer to the SiC valence band maximum, hence the a possible explanation/reason for fluorine termination rather than hydrogen termination of SiC surfaces.

E. Conclusions

In conclusion, a completely dry process which removes carbon contamination from $(0001)_{Si}$ 6H-SiC surfaces via UV/O_3 oxidation and removes surface oxides via HF vapor exposure has been demonstrated. Based on the levels of non-carbidic carbon and oxide surface contaminants, this dry cleaning procedure has been found to be equivalent to or better than other standard wet chemical processes. Contrary to silicon, the HF vapor exposure is observed to leave a fluorine terminated SiC surface as opposed to a hydrogen terminated SiC surface.

F. Future Research Plans and Goals

HF vapor and UV/O_3 cleaning of $(000\text{-}1)_C$ 6H-SiC will be investigated. In addition, investigation will be conducted of other processes which could lead to better hydrogen or fluorine termination of (0001) 6H-SiC.

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III. Design and Construction of Silicon Carbide Chemical Vapor Deposition System

A. Introduction

A silicon carbide system is being built in order to grow silicon carbide thin films of high quality. A design has been developed. Most parts have been received and have been assembled, and construction is currently under way on the electrical and gas lines.

B. Experimental Procedure

The system design is comprised of a six-way cross, serving as a loadlock, from which the growth and the reflection electron diffraction (RHEED) chambers are attached. Both chambers are perpendicular to the axis of the loadlock. The sample will be transferred to and from the various chambers on a SiC coated graphite susceptor platform on which the sample will be placed. The transfer mechanism consists of a platform which is moved from chamber-to-chamber by means of a manipulator rod, which is screwed to the side of the susceptor.

The growth chamber consists of a rotating module to which the susceptor is attached. Film growth will be achieved with the sample inverted, i.e., with the gases flowing upward while the susceptor is rotated. The susceptor is attached to the rotating rod assembly by a groove into which the susceptor slides when transfer of the sample occurs. Once the sample is transferred to the rotating rod, the latter is moved down to the quartz portion of the reaction chamber. Here, the sample is heated via RF coil, and gases are introduced from the bottom of the reactor. Growth temperatures will be monitored via a standing pyrometer mounted outside the quartz chamber and aimed at the sample. Growth processes, such as gas flow rate and pressure, will be monitored electronically. Gas flow rates will be controlled by mass flow controllers, and pressure by capacitance manometers.

The RHEED will be employed to monitor film crystallinity, crystal structure and the formation of new surfaces. Since the growth of high-quality crystalline SiC films is the primary goal, a RHEED chamber which is attached to a nominal high vacuum system to prevent direct exposure to atmosphere after growth will be useful to characterize the surface structure of the films.

The SiC growth process will employ SiH_4 and C_2H_4 as the reactive components carried in a H_2 diluent. Nominal flow rate will be on the order of 1 to 10 sccm for each reactant. Flow rates of H_2 will be on the order of $\cong$3 liters per minute. Other gases which will be included on the system will be NH_3 and an N_2/H_2 mixture for doping and Ar. Triethylaluminum will also be used for doping which will be maintained at a constant temperature by a heater bath.

C. Results

Accomplishments to date include the following: 1) stainless steel chambers for sample transfer, growth, and RHEED analysis as well as a support frame have been designed and

fabricated for the system; 2) three, six-way crosses have joined with the associated gate valves on the frame, and available flanges and window ports have been attached; 3) a quartz chamber-to-cross assembly has been machined which will provide a sealed interface between two parts of the growth chamber; 4) quartz cylinders have been cut to design dimensions; 5) flange parts, pressure gauge attachments, pump connection parts, and a rotating rod assembly, have been machined; 6) an RF generator has been refurbished to provide RF heating to the susceptor; 7) the assembly of a switch panel to control the nupro valves and to enable computer control has been completed; 8) a RHEED chamber manipulator has being fitted with a holder which will accommodate the susceptor upon transfer; 9) electrical wiring of the switch panel to control the gas inlet valves has been assembled; 10) various gas lines have been assembled on a panel and 11) installation of electrical and water utilities for the system, as well as safety changes in the laboratory, have been requested.

D. Discussion

The proposed design was developed with many sources of input. A number of constraints determined the design configuration and materials used in the system. One of the main concerns was the high operating temperature of the growth chamber. Since temperatures in the range of 1600-1700°C will be used to grow the SiC thin films, it was determined that quartz would be the best material for the growth portion of the chamber. Once this was determined, a design had to be developed to cool the chamber. A double-walled quartz vessel, water cooled around the perimeter, was determined to be the optimum design for cooling.

Another concern was the transfer mechanism of the susceptor and the placement of samples on the susceptor surface. It was determined that small silicon carbide screws would be the most flexible for our purposes to accommodate various sized samples. For the transfer mechanism, a simple tongue-in-groove assembly, moved between chambers by means of a transfer arm which would screw into the side of the susceptor, was deemed most simple and practical.

E. Conclusions

A system design for the deposition of SiC thin films has been developed. Most components have been either received or are in transit. Other needed parts are currently being machined. Further assembly of the system is expected when electrical and water sources to the laboratory enable us the start up of many parts of the system.

IV. Growth of AlN and SiC by Molecular Beam Epitaxy

A. Introduction

Thin films of SiC and AlN, two important materials in current semiconductor research, have been recently grown by molecular beam epitaxy (MBE) under this program [1,2]. A partial list of the results from these studies include the following: i) Single-crystalline films of 3C-SiC(111) and 6H-SiC(0001) were grown on 6H-SiC(0001) substrates. Polytype and growth rate were controlled by substrate orientation, substrate temperature and gas phase chemistry [3]. ii) Single-crystalline AlN films were deposited on vicinal and in 6H-SiC(0001) wafers using aluminum evaporated from an effusion cell and reactive nitrogen derived from either a electron cyclotron resonance plasma source or NH_3. In general AlN films <50 Å had higher defect density on vicinal 6H-SiC than on nominally on-axis 6H-SiC. iii) Single-crystal heterostructures and solid solutions of AlN and SiC were also achieved. Superior AlN/SiC multilayers were realized when very thin AlN layers were deposited on on-axis 6H-SiC substrates. Single-phase solid solutions of AlN_xSiC_{1-x} were deposited for $0.2< x <0.8$. A transition from the zincblende to the wurtzite structure was observed at $x = 0.25$ [4].

The MBE system has recently been upgraded, as discussed in Section B: *Experimental Procedure*. The new experiments now being conducted are described in Section C: *Future Research Plans and Goals.*

B. Experimental Procedure

Prior to growth, the SiC substrates are cleaned using *ex situ* and *in situ* procedures developed in the group and previously reported [2]. The crystallography of the substrate surface before growth is determined by reflection high energy electron diffraction (RHEED). Film growth is conducted in a vacuum chamber with an ultimate base pressure below 1×10^{-9} Torr. Substrates of 6H-SiC(0001) are inserted into the chamber through a load-lock which can be evacuated to a pressure below 1×10^{-8} Torr. The SiC films are grown by gas-source GSMBE using SiH_4 and C_2H_4. The gas-flows are accurately controlled by regulating the pressure over a flow-cell. Films of AlN are grown via evaporation Al from an effusion cell simultaneous with the introduction of NH_3 through a mass flow controller. The gases of H_2, N_2 and Ar may also be introduced during growth.

The GSMBE system is equipped with two *in situ* analysis tools. The gases in the chamber are monitored with a Leybold H100M residual gas analyzer (RGA). Differential pumping of the RGA allows the gas content in the chamber to be measured at pressures above 1×10^{-3} Torr. The surface structure can be analyzed with (RHEED).

In addition to these *in situ* techniques, several *ex situ* analysis techniques are available including transmission electron microscopy (TEM), X-ray diffraction (XRD) and scanning

electron microscopy (SEM) for structural and microstructural investigations; Auger electron spectroscopy (AES) and secondary ion mass spectroscopy (SIMS) for chemical analyses; and capacitance-voltage (C-V), current-voltage (I-V) and Van der Pauw Hall measurements for electrical characterization.

C. Future Research Plans and Goals

1. Growth of high-quality SiC thin films and heterostructures and solid solutions of SiC and AlN.
2. Investigations regarding the mechanisms controlling the surface chemical effects of H_2 on SiC growth rate and polytype change (3C - 6H or 4H) will be investigated as a continuation of the recent works by Kern *et al.* [3]. The growth of 6H-SiC on 3C-SiC and total polytype control will be studied.
3. The growth of SiC on 2H-AlN will be investigated. The achievement of 2H-SiC will be a primary goal in these experiments.
4. Growth of heterostructures from 6H- (and 4H-) SiC/3C-SiC and AlN/SiC, using the results and experience from the foregoing investigations as input for the experiments.
5. Growth of high quality AlN layers as a high temperature dielectric on SiC. The effect of H_2 and NH_3 on the AlN/SiC interface will be determined.
6. Detailed studies of the growth and structural changes in AlN_xSiC_{1-x} solid solutions will be conducted as a function of AlN concentration as a continuation of the recent investigations by Kern *et al.* [4].
7. Investigation regarding the use of the AlN/SiC heterostructures and the solid solutions as buffer layers on which to grow AlN and SiC thin films.

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V. Rectifying and Ohmic Contacts for P-type Alpha (6H) Silicon Carbide

A. Introduction

The fabrication ohmic contacts to 6H-SiC which have low specific contact resistivity and good thermal stability remains a serious challenge to the advancement of SiC device technology. For SiC power devices to have the advantage over Si, the contact resistivities must be below 1×10^{-5} Ω-cm^2 [1]. The thermal stability of ohmic contacts is of particular concern for p-type SiC, which yields substantially large Schottky barrier heights (SBHs) with transition metals. The technology has traditionally relied on Al-based metallization to dope the SiC surface below the contacts as a result of annealing. While the fabrication of ohmic contacts to SiC has depended on very heavily-doped surfaces, the large SBHs associated with metals on p-type SiC limit the achievable contact resistivities. Based on all of these issues and experiments already performed at NCSU, our goals are to produce contacts which are thermally stable, oxidation resistant and have low contact resistivities.

Low resistance contacts to p-type SiC remain a substantial challenge for high temperature and high-power devices. An Al-Ti alloy [2] annealed at 1000°C for 5 min. was reported to yield contact resistances ranging from 2.9×10^{-2} Ω cm^2 for a carrier concentration of 5×10^{15} cm^{-3} to 1.5×10^{-5} Ω cm^2 for 2×10^{19} cm^{-3}. The thermal stability of these contacts was not reported. Aluminum deposited on a heavily-doped 3C-SiC interlayer on a 6H-SiC substrate and subsequently annealed at 950°C for 2 min. reportedly yielded contact resistivities of $2–3\times10^{-5}$ Ω cm^2 [3]. Because of its low melting point (660°C), however, pure Al would be unsuitable for high temperature applications. Platinum contacts annealed from 450 to 750°C in 100°C increments were also used as ohmic contacts to p-type SiC [4]. These contacts, which rely on the combination of a highly-doped surface and the high work function of Pt, have not been known to yield contact resistivities as low as those for contacts containing Al.

This report compares the electrical and chemical characterization of annealed Al-based (NiAl) and B-based (Cr-B) contacts on p-type 6H-SiC. In particular, the current-voltage characteristics and oxidation properties were investigated before and after annealing at 1000 °C. In addition, the electrical properties of Schottky contacts on p-type SiC were measured and compared to typical behavior found previously for Schottky contacts on n-type SiC.

B. Experimental Procedure

Vicinal, single-crystal 6H-SiC (0001) wafers provided by Cree Research, Inc. were used as substrates in the present research. The wafers were doped with N or Al during growth to create n- or p-type material, respectively, with carrier concentrations of $1–5\times10^{18}$ cm^{-3}. Homoepitaxial layers (1–5 μm thick) grown by chemical vapor deposition (CVD) were Al-doped with carrier concentrations ranging from 1×10^{16} to 1×10^{19} cm^{-3}. The surfaces were

oxidized to a thickness of 500–1000 Å in dry oxygen. The substrates were cleaned using a 10 min. dip in 10% hydrofluoric acid, transferred into the vacuum system, and heated at 700°C for 15 min. to remove any residual hydrocarbon contamination.

A UHV electron beam evaporation system was used to deposit the NiAl, Ni, Au, Pt, and Cr-B films. After depositing 1000 Å of NiAl, 500–1000 Å of Ni was deposited as a passivating layer. Pure Ni (99.99%) and pure Al (99.999%) pellets were arc melted to form alloyed pellets of 50:50 atomic concentration for evaporation of NiAl. The films were deposited onto unheated substrates at a rate of 10–20 Å/s. Chromium and B were evaporated simultaneously from separate evaporation sources. The pressure during the depositions was between 5×10^{-9} and 5×10^{-8} Torr.

Circular contacts of 500 μm diameter were fabricated for electrical characterization by depositing the metal films through a Mo mask in contact with the substrate. Silver paste served as the large area back contact. For contact resistance measurements, TLM patterns [5] were fabricated by photolithography. The Ni/NiAl films were etched in phosphoric acid : acetic acid : nitric acid (12 : 2 : 3) at 50°C (etch rate ≈ 30 Å/s). The contact pads were 300×60 μm with spacings of 5, 10, 20, 30 and 50 μm. Mesas in the substrate were not fabricated. All annealing was conducted in a N_2 ambient in a rapid annealing furnace.

Electrical characteristics were obtained from current-voltage and capacitance-voltage measurements. Current-voltage (I-V) measurements were obtained with a Rucker & Kolls Model 260 probe station in tandem with an HP 4145A Semiconductor Parameter Analyzer. Capacitance-voltage (C-V) measurements were taken with a Keithley 590 CV Analyzer using a measurement frequency of 1 MHz.

Auger electron spectroscopy (AES) was performed with a JEOL JAMP-30 scanning Auger microprobe. The films were sputtered with Ar ions at a beam current and voltage of 0.3 μA and 3 kV, respectively, to obtain composition profiles through the thickness of the films.

C. Results and Discussion

Chemical Characterization of As-deposited Films. An Auger depth profile of a film deposited from the NiAl source showed that the overall composition remained relatively stable. The relative compositions of Ni and Al were calculated by referencing to pure Ni and pure Al standards and accounting for their corresponding sensitivity factors. The average atomic composition was approximately 50:50. With reference to Cr and B standards, the first Cr-B film co-deposited by e-beam evaporation was determined to be comprised of approximately 20% Cr and 80% B (CrB_4). While a thin oxide layer was detected at the surface of the NiAl film, no O was detected within either of the films. After recalibrating the thickness monitors for Cr and B, films were deposited with an intended composition of CrB_2.

Schottky Contacts. In the as-deposited condition the Ni/NiAl contacts were rectifying on p-type SiC with carrier concentrations of 1.6×10^{16} and 3.8×10^{18} cm^{-3} in the epilayer. The sample with the lower carrier concentration displayed leakage current densities of ~1×10^{-8} A/cm^2 at 10 V and ideality factors between 1.4 and 2.4, while the latter sample displayed approximately five orders of magnitude higher leakage current densities and similar ideality factors. The average Schottky barrier heights (SBH's) calculated for the samples with the lower and higher carrier concentrations were 1.37 and 1.26 eV, respectively. The lower SBH calculated for the former sample is likely due to enhanced thermionic field emission through the upper energy region of the barrier because of the narrower depletion region. Hence, the 1.37 eV value is believed to be more accurate.

Similar results were obtained for as-deposited Ni, Au, and Pt contacts on p-type ($2.1–4.5\times10^{16}$ cm^{-3}) 6H-SiC (0001). These samples displayed similar leakage currents and ideality factors of 1.3–2.1 and <1.1, respectively. From these measurements SBH's of 1.31 eV for the Ni contacts and 1.27 eV for the Au contacts were calculated. In comparison, as-deposited Ni on n-type (4.1×10^{16} cm^{-3}) 6H-SiC (0001) yielded ideality factors below 1.1, similar leakage current densities to those stated above, and SBH's of 1.14 eV and 1.21 eV calculated from I-V and C-V measurements, respectively.

Our measurements on p-type SiC have shown consistent differences from measurements on n-type 6H-SiC. The SBH's tended to be higher on p-type than on n-type material. While leakage currents for Au, NiAl, and Ni contacts on p-type 6H-SiC were comparable to Ni contacts on n-type 6H-SiC, the ideality factors were higher on p-type SiC. These ideality factors and SBH's are higher than for Ni contacts (and other previously studied contacts) on n-type 6H-SiC (0001). The higher ideality factors indicates that thermionic emission was not the dominant current transport mechanism in the p-type SiC and may indicate the occurrence of recombination at deep levels.

Conversely, the relationship between the SBH's of the metals on p-type SiC and their respective work functions was similar to that which we previously found for n-type SiC. The calculated SBH's on p-type SiC are plotted vs. the metal work functions in Fig. 1. The work function for NiAl was taken to be the average of the work functions for pure Ni and pure Al since a value was not found in the literature for NiAl. The slope of the line fit to the empirical data was -0.28 as compared to a slope of -1.0 for the theoretical data. These results indicate that surface states on p-type 6H-SiC (0001) cause a partial pinning of the Fermi level, in agreement with the results of our previous, extensive study on n-type SiC.

Ohmic Contacts. The Ni/NiAl contacts were sequentially annealed for total times of 10–80 s at 1000 °C in a N_2 ambient. This temperature was used because (1) limited intermixing of Al and SiC was reported at 900°C [6] and (2) other papers report annealing in this

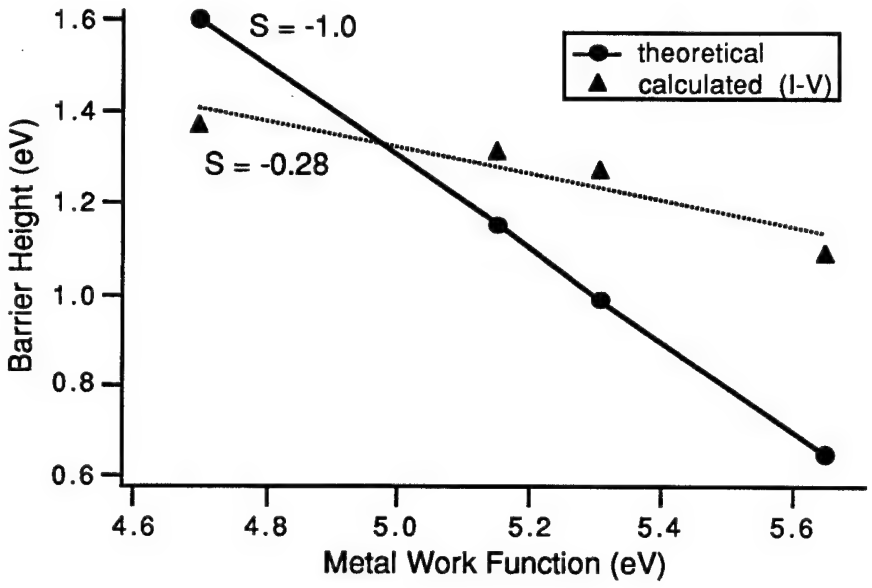

Figure 1. Graph of calculated and theoretical barrier heights of as-deposited NiAl, Au, Ni, and Pt contacts on p-type 6H-SiC vs. metal work function. The calculated values were determined from I-V measurements, and the theoretical values were calculated according to the Schottky-Mott limit. The slopes, S, of the lines fit to each set of data are indicated on the graph.

temperature range for Al-based ohmic contacts on p-type SiC [2,3,7]. Because of the extremely high thermodynamic driving force for Al to form an insulating oxide layer (ΔG_f (Al_2O_3) ~ -1300 kJ/mol at 1000 °C [JANAF - Chase, M., et al., JANAF Thermochem. Tables, 3d Ed. J. Phys. Chem. Ref. Data, 1985. 14(Supp. 1)]), 1000 Å of Ni was deposited on top of the NiAl contacts to slow the oxidation process.

The calculated specific contact resistivities of Ni/NiAl on p-type SiC (1.5×10^{19} cm^{-3} in the epilayer) after annealing at 1000°C (Ar ambient) for 20, 40, 60, and 80 s were 2.0×10^{-2}, 1.9×10^{-2}, 2.2×10^{-2}, and 3.1×10^{-2} Ω cm^2, respectively. The additional force on the probes needed to obtain consistent results indicates that an oxide began to form at the surface which would likely cause more severe problems if the samples were annealed further. The increase in contact resistivity is believed to be due to the surface oxide layer.

An Auger depth profile (Fig. 2) of Ni/NiAl/SiC annealed at 1000°C for 80 s in Ar shows that a surface oxide formed during the annealing process. After sputtering for a couple of minutes, the O concentration dropped to below detectable limits; however, the data shows a decreasing Al concentration in the direction toward the SiC interface. This indicates that the kinetics are more favorable for the Al to diffuse toward the surface and react with O than for the Al to react with the SiC. Some of the Ni has probably reacted with Si at the interface to form a silicide, as indicated by the local maximum in the Ni intensity near the SiC interface, while the peak in the C intensity indicates the presence of an adjacent C-rich layer.

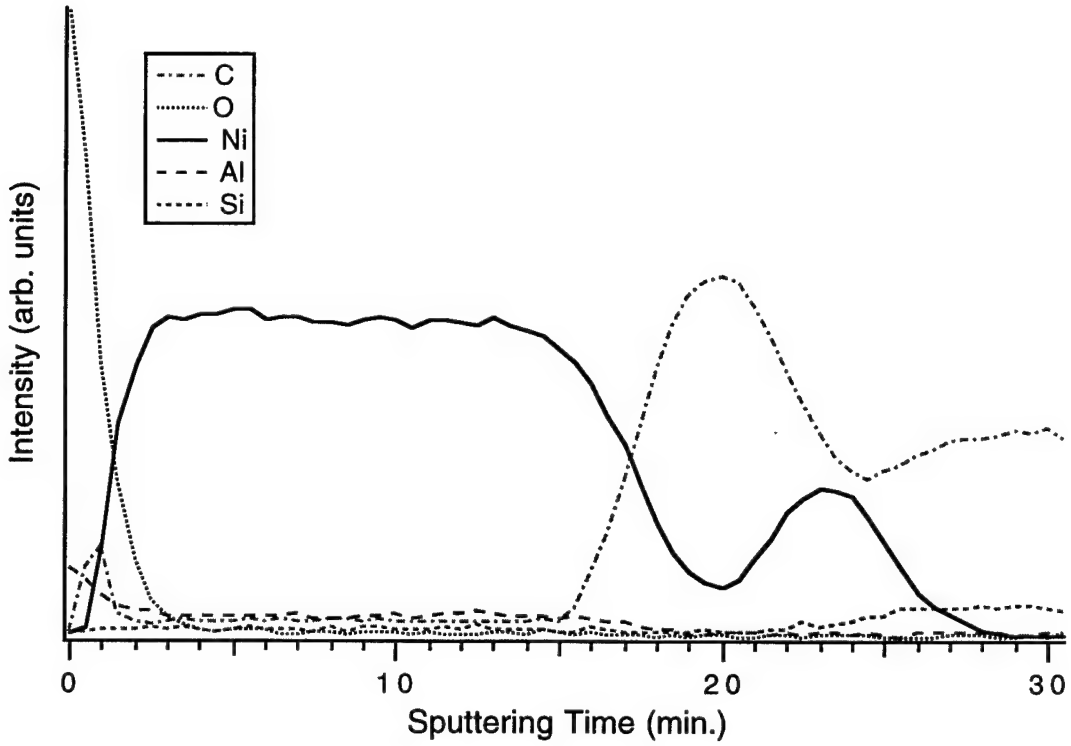

Figure 2. AES composition profile of Ni (1000 Å) / NiAl (1000 Å) / 6H-SiC annealed at 1000 °C for 80 s in N_2.

The demonstrated oxidation problem with Al necessitates the development of ohmic contacts which do not consist of substantial concentrations of Al. To reduce this problem we have chosen to investigate contacts which contain B.

The main reasons for choosing B are that it is also a p-type dopant in SiC, its oxide is not as stable, and it is a much faster diffusant in SiC. Table I compares some important properties of B, Al, and their associated oxides. Recent reports [8-10] show that the 'shallow' activation energy for B in SiC is significantly less than previously reported. Boron compounds tend to be more stable at high temperatures than aluminum compounds which suffer from the low melting point of Al. Also, the diffusion coefficient of B is at least three orders of magnitude greater than that of Al. Therefore, more B than Al will diffuse into the SiC at lower temperatures. As discussed in this report, a major problem with Al-based contacts is the strong driving force for forming an insulating oxide layer. This situation is shown by the extremely low equilibrium partial pressure of oxygen, p_{O2}, for Al_2O_3 formation. While B_2O_3 also has a low p_{O2}, it is significantly higher than that for Al_2O_3, indicating that the driving force for B to form an oxide is significantly lower. There is also a larger number of metals which would reduce the oxide formed with B than that formed with Al, a fact which is encouraging when one is trying to diffuse free B into SiC. Another advantage is that the melting point of boron oxide is notably low. Several boron compounds which possess reasonably low resistivities and high melting temperatures are listed in Table II. We have chosen to investigate Cr-B contacts because of the

Table I. Selected Properties of B, Al, and Associated Oxides

Element	Activation Energy in 6H-SiC (meV)	Solid Source Diffusion, DSiC @ 1800°C (cm^2/s)	Equilibrium Partial Pressure of O_2, pO_2 @ 700°C (Torr)	Melting Temp. of the associated oxide, T_{melt} (°C)
B	300 [8-10]	10^{-11} [11-12]	10^{-35}	450
Al	200 [9]	$<10^{-14}$ [13]	10^{-47}	2040

relative ease to deposit these materials by electron beam evaporation and the demonstrated use of Cr in metallization schemes for diffusion barriers. The refractory nature of these materials increases the probability of forming ohmic contacts which will be stable at high temperatures.

Cr and B were simultaneously deposited on p-type (~1×10^{18} cm^{-3}) 6H-SiC epitaxial layers. A thermally grown oxide layer was removed in a 10% HF aqueous solution. The as-deposited contacts for the sample with a carrier concentration of 1×10^{18} cm^{-3} displayed rectifying behavior with low leakage currents (~4×10^{-8} at 10 V) and ideality factors between 1.5 and 1.9. Rectification was expected since the contacts had not been annealed, and large SBH's normally exist for as-deposited contacts on p-type SiC.

The samples were annealed at 1000°C for total times varying from 60 to 300 s in an Ar ambient (Fig. 3). After 60 s at 1000°C, the contacts showed substantial changes in their electrical characteristics. With an increase in annealing time to 240 s, the contacts became more ohmic-like. However, after annealing for 300 s, the contacts became rectifying with high leakage currents; this result may be due to the formation of B_4C at the interface.

Although true ohmic behavior of Cr-B contacts has not yet been achieved, the improved oxidation resistance over that of the NiAl contacts in combination with the tendency toward ohmicity displayed in nonimplanted samples annealed at 1000°C for 60–240 s makes the former contacts a potentially beneficial alternative to Al-based metallization. Higher surface carrier concentrations in the SiC epilayers and ion implantation of Al or B should improve the ohmic behavior of the contacts. (Capacitance-voltage measurements of the SiC showed an initial decrease in the carrier concentration profile towards the surface, likely due to depletion of Al during oxidation; however, because of the finite depletion width established from the Hg contact used in the measurement, the carrier concentration at distances less than 300 Å from the surface could not be measured.) Figure 4 shows an AES depth profile of Cr-B/SiC annealed at 1000°C for 360 s in Ar. The O signal diminished to below detectable limits after sputtering for approximately 10 s. The finite O level indicated in the profile is attributed to the tailing of the Cr peak due to overlapping energy windows for measuring the two peaks. No O peak was observed after sputtering into the film.

Table II. Resistivities and Melting Points of Selected Boron Compounds

Material	Electrical Resistivity (μΩ cm) @ 298 K [14]	Melting Temp. (°C) [15]
B	18×10^{11}	2092
CrB_2	30	2200
GdB_4	31	2650
MoB	45	2600
NbB_2	26	3000
TaB_2	33	3037
VB_2	23	2747
ZrB_2	10	2972

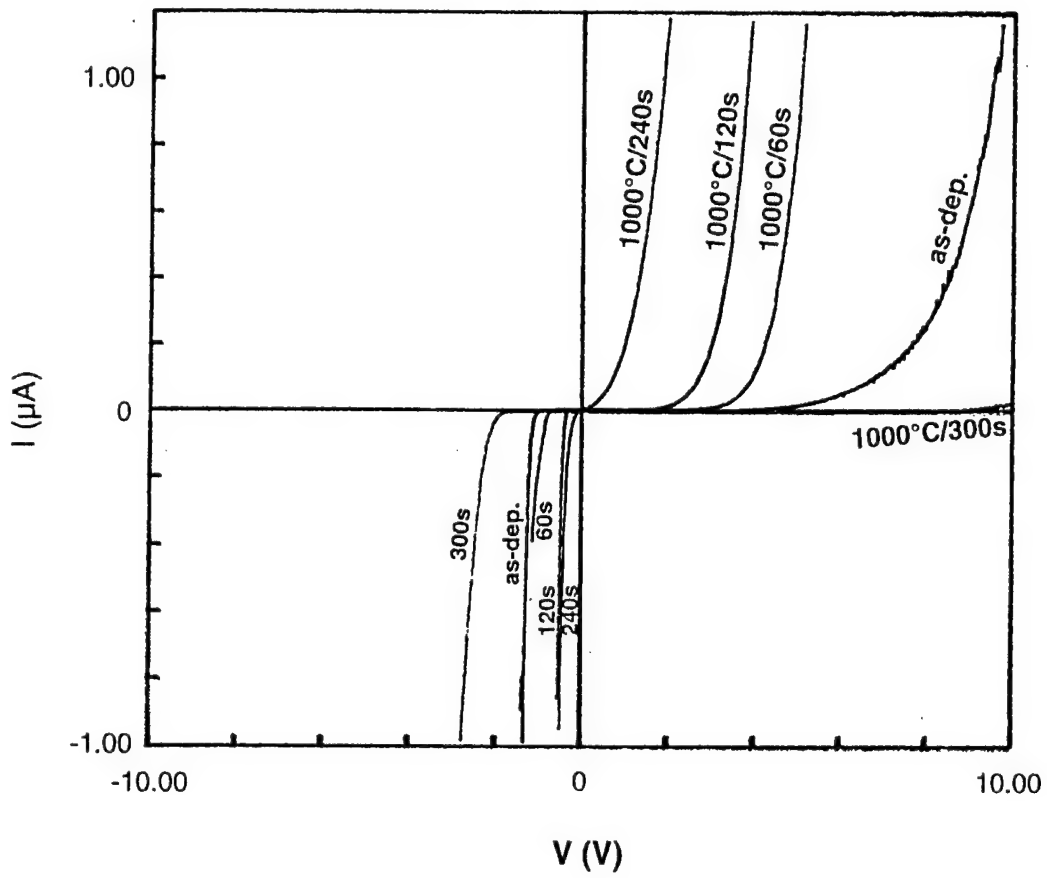

Figure 3. Current-voltage (I-V) characteristics of Cr-B on p-type 6H-SiC as a function of annealing time at 1000 °C in Ar.

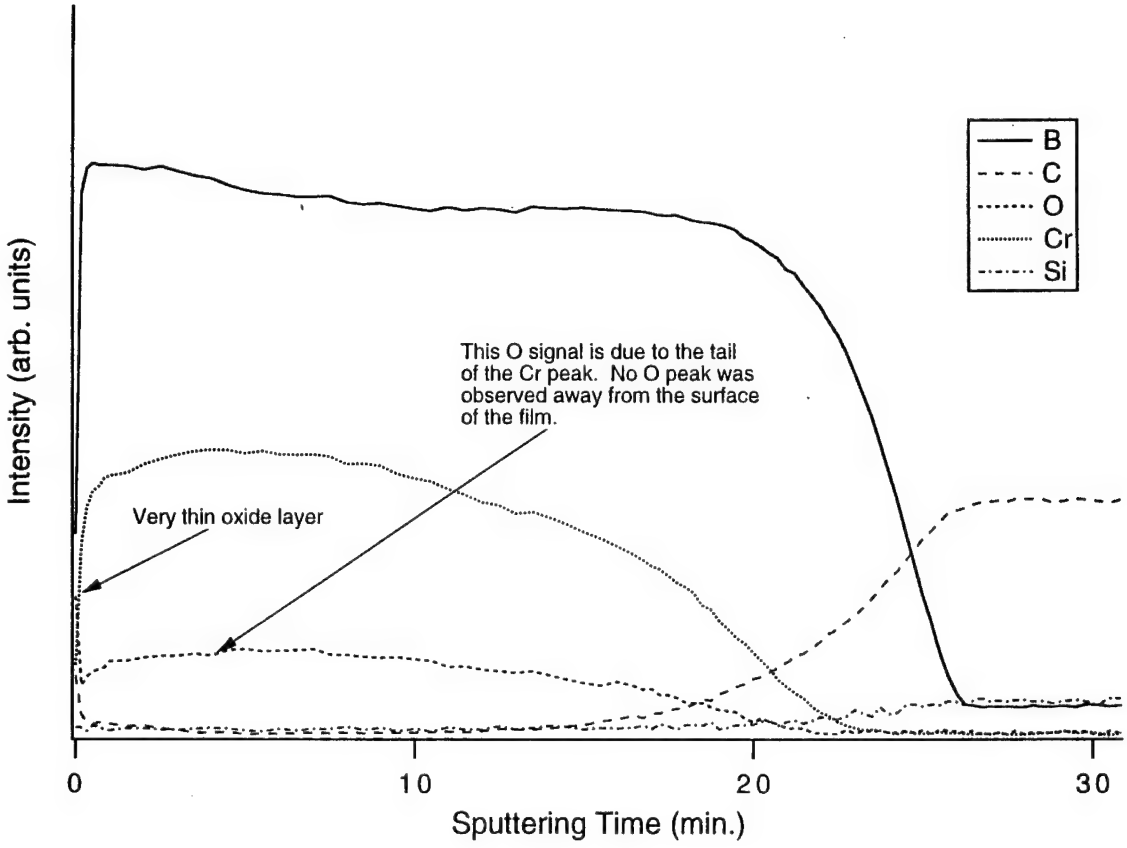

Figure 4. AES composition profile of Cr-B / 6H-SiC annealed at 1000 °C for 300 s and 1100 °C for 360 s in Ar.

D. Conclusions

Nickel-aluminum was investigated primarily as an ohmic contact for p-type 6H-SiC because of the p-type doping of Al in SiC, the high melting point of NiAl (as compared to Al), and the tendency of Ni to form silicides but not carbides. This latter property potentially could have resulted in extraction of Si from the SiC lattice in exchange for Al, thereby enhancing the p-type carrier concentration at the surface. Although the I-V measurements indicate that some Al may be diffusing into the SiC after the longest annealing time performed (80 s at 1000°C), this potential for reaction between Al and SiC appears to be exceeded by the driving force for Al to diffuse to the surface and react with O. A concentration profile obtained from AES analysis shows that Al has diffused through the 1000 Å Ni overlayer to form a thin (200 Å estimated) oxide layer.

In addition to the ohmic behavior resulting from annealing the NiAl contacts, as-deposited Ni, NiAl, and Au contacts deposited at room temperature on p-type ($N_A < 5\times10^{16}$ cm^{-3}) 6H-SiC (0001) were rectifying with low leakage currents, ideality factors between 1.3 and 2.4, and SBH's of 1.31, 1.27, and 1.37 eV, respectively. These results indicate that the Fermi level is partially pinned at p-type SiC surface, in agreement with our previous results on n-type SiC.

As an alternative to Al for fabricating ohmic contacts to p-type 6H-SiC, Cr-B was investigated because of its low resistivity, high melting temperature, high diffusivity of B in SiC, and reduced tendency for oxidation (compared to that of Al). In the as-deposited condition these contacts were rectifying with low leakage currents. After annealing at 1000°C for 60 s, the contacts displayed semi-ohmic behavior and became less resistive with successive 60 s anneals to a total time of 240 s. The contacts showed rectification after annealing for 300 s, a result which may be associated with the formation of B_4C at the interface. C-V measurements indicated that the surface carrier concentration was less than the average carrier concentration in the SiC epilayer due to the thermal oxidation process; a low surface carrier concentration degrades the ohmicity of the contacts. Thus, these contacts deposited on unoxidized, ion implanted (with Al and/or B) SiC will be investigated. The most promising result was the substantially improved oxidation resistance.

E. Future Research Plans and Goals

Ion implantation of Al and/or B at elevated temperatures (~850°C) into p-type SiC will be performed to enhance the carrier concentration at the surface. The atomic concentration profiles and carrier concentrations will be characterized by secondary ion mass spectroscopy (SIMS) and capacitance-voltage (C-V) measurements, respectively. The electrical properties of the Cr-B contacts will be characterized as a function of both surface carrier concentration and annealing conditions. Contact resistivities will be calculated from transmission line model (TLM) measurements to optimize the processing conditions. Samples have been prepared for TEM studies to identify phases formed at the interfaces after annealing and to use as feedback for the optimization process.

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VI. Development of a System for Integrated Surface Cleaning and Oxide Formation on 6H-SiC

A. Introduction

The development of high-temperature, -power and -frequency devices based on SiC requires a complete understanding of the oxide formation and interface characteristics. To have SiC device technology introduced into the mainstream industrial community, it is necessary that current technologies be employed to device fabrication. Thermal oxidation of p-type SiC has led to an increase in defects that have resulted in degradation of the electrical properties. An oxide positive space charge has been estimated to be about 1.5×10^{12} cm^{-2}, and the estimation of fast interface states is of the same order [1]. It is proposed that the Al dopant on p-type SiC is more readily redistributed in SiO_2, while the N dopant on n-type is not. This yields significant quantities of Al in thermally grown oxides on p-type SiC that form Al_2O_3, which may increase the number of defects in the oxide and the SiO_2/SiC interface [2]. The resultant oxide displays an increase in space charge, a lowering of the breakdown voltage, and an increase in both fast and slow interface state densities. By using an integrated UHV system, interfaces with lower contaminant levels will be prepared while gaining a better understanding of the SiC oxide formation process. The UHV compatible surface preparation and oxide formation system will be integrated with an advanced system that includes other processing and characterization capabilities that will allow for *in vacuo* characterization of the SiO_2/SiC interface followed by *ex situ* electrical characterization. From recent experiments on SiC, it was shown that the cleaning and surface preparation of SiC is more involved than Si [3]. In order to completely remove oxygen from the SiC surface, a Si capping layer was deposited and then thermally desorbed. This removed the oxygen within the detection limits of AES and XPS. It is unclear at this point whether it is necessary to totally remove all the oxygen from the SiC surface. It is proposed that the residual oxide from most surface preparation techniques is oxygen trapped at near-surface grain boundaries [4]. A systematic approach is underway to develop a process that will yield an electrical quality oxide on SiC.

B. Experimental Approach

The integrated system will allow for most of the characterization to be accomplished without exposing samples to the ambient. Furthermore, the processes will be characterized at various stages, thus allowing for the understanding of the entire oxidation process. A typical process is given as follows: (1) surface preparation; (2) initial insulator formation; (3) CVD insulator deposition. A schematic of the process is shown in Fig. 1. At each of these stages, there are a wide variety techniques are available.

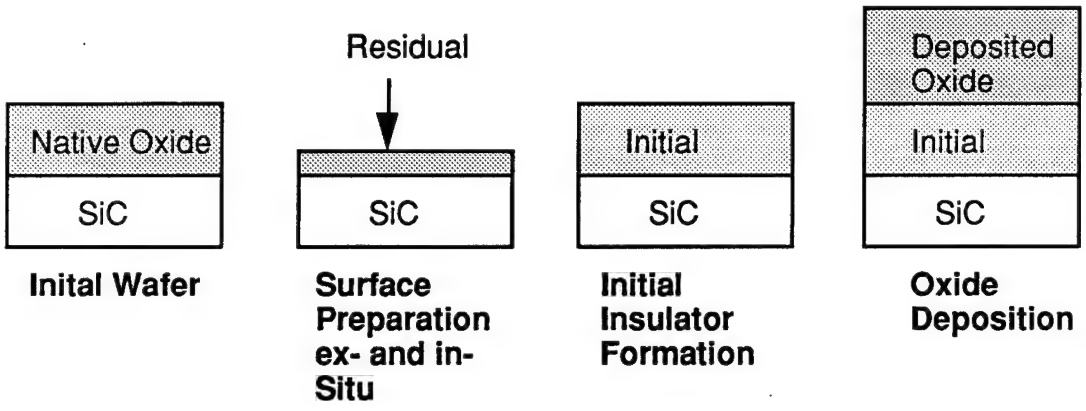

Figure 1. Basic process for insulator formation on SiC.

An experimental matrix has been set up to provide a systematic approach to the insulator formation process. Table I lists the procedures and processes that will be used to determine the SiC/SiO_2 interface and deposition process. The base line procedure is a RCA clean followed by thermal oxide growth. The base line procedure will be compared to all other procedures. *Ex situ* surface preparation will be the first process investigated. Once the *ex situ* surface preparation technique that yields the highest quality thermal oxide has been determined, it will become the standard procedure. Using the *ex situ* preparation process previously determined as a standard process the *in situ* surface preparation will be investigated. The *in situ* process(es) that again yield the highest quality thermal oxide will be added as a standard preparation procedure. Initial insulator formation is then investigated using the previous *ex situ* and *in situ* surface preparation techniques. Once an initial insulator formation procedure that yields a higher quality oxide is determined, it will become part of the standard preparation/growth techniques. This systematic approach will investigate the various processes and chemistries that are present in the oxidation of SiC and the SiC/SiO_2 interface.

Surface preparation is arguably the most important step to high-quality insulator growth. Ensuring a clean smooth surface is necessary for oxide growth. Some of the various

Table I. Experimental Matrix for High-quality Insulator Formation on SiC

Ex Situ	*In Situ*	Initial Oxide	Insulator Deposition
RCA	None	None	Thermal CVD
RCA/HF	H-plasma	Thermax oxidation	Plasma CVD
RCA & pH Controlled HF	H/SiH_4 Plasma	Plasma Oxidation	
RCA/HF/UV Ozone	Excess Si/Thermal Anneal		
RCA/Nitric	(HF Vapor)		

procedures are: (1) wet chemical clean ; (2) plasma cleaning; and (3) HF vapor phase. Current cleaning techniques have been developed that will yield various levels of cleaning, specifically, most procedures cannot remove all oxygen from the SiC surface. Hydrogen plasma cleaning removes surface contaminants, but as shown in Fig. 2, leaves the residual oxide after the HF dip. Likewise, a H/SiH_4 plasma has be shown to etch SiO_2 on Si [5] but is unable to remove the residual oxide on SiC. This is demonstrated by the Auger Spectrum in Fig. 3.

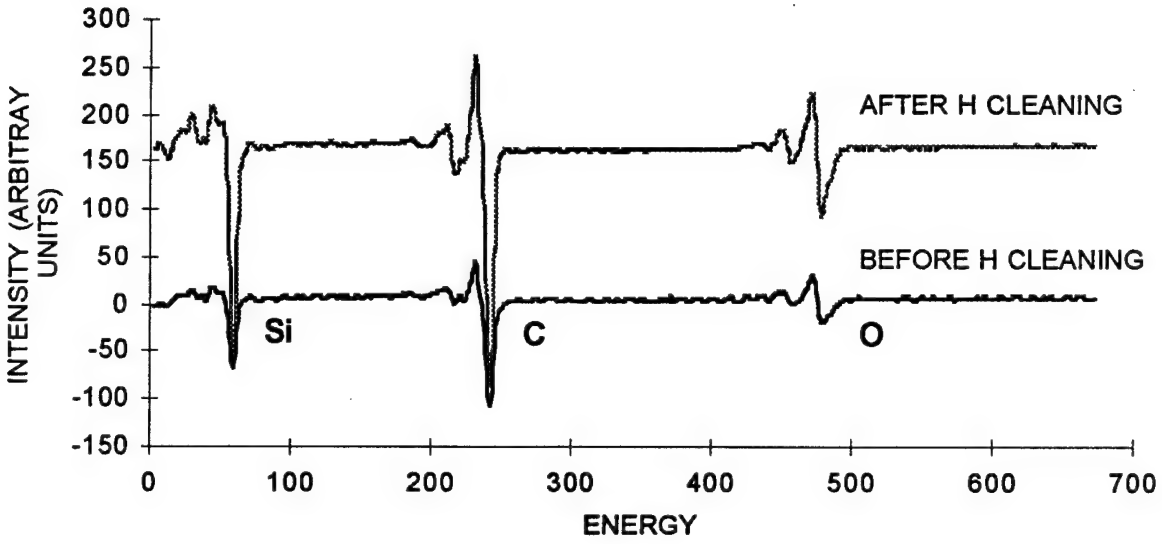

Figure 2. AES spectrum of 6-H SiC before and after H-plasma cleaning.

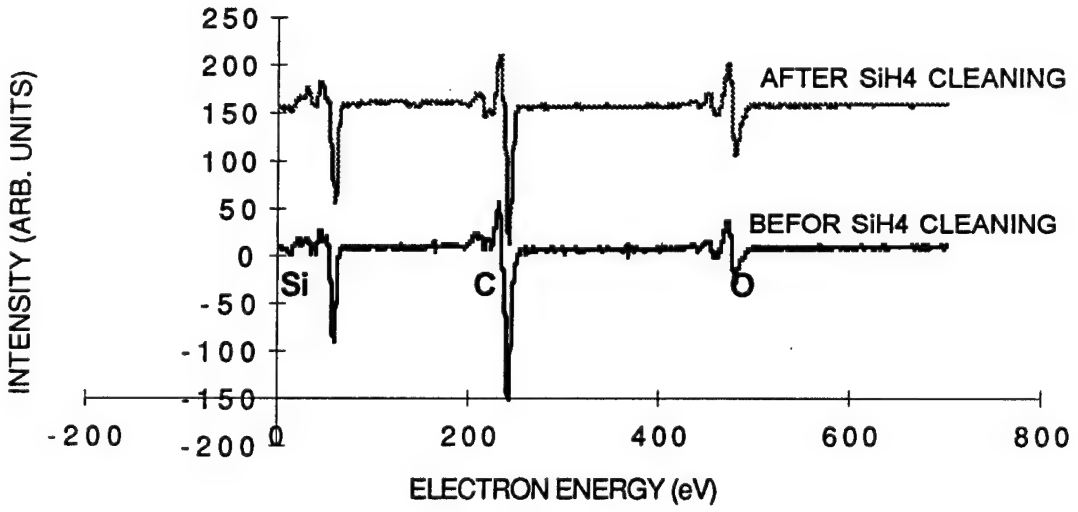

Figure 3. AES spectrum of 6-H SiC before and after H/SiH_4 plasma cleaning.

It has not been established if this residual oxide on the SiC will result in a degradation of the electrical performance of insulators grown on it. Further investigation into the effect that the residual oxide will have on electrical characteristics is needed. As shown in previous experiments [1], it is possible to remove all the oxygen contamination within detection limits.

Insulator formation on SiC is where some of the major problems are manifested. On p-type SiC there is considerable dopant redistribution and defect formation during the transition region between SiC/SiO_2 in thermally grown oxides. Which process or combination of processes will minimize defect formation, dopant redistribution, and maximize the electrical properties on the initial oxide formation will be observed by using diverse techniques for initial insulator formation and deposited oxides. Some of the procedures are: (1) UV ozone; (2) nitric bath; (3) plasma enhanced CVD (PECVD). CVD insulator formation is the final step in the oxide formation process in which oxide is deposited on the initial oxide to the desired thickness. This process is proposed to limit redistribution of dopants on p-type SiC. Deposited oxides do not have as desirable dielectric constants and can have considerable interface densities. By growing an initial oxidation layer, it is intended that the interface densities will be minimized, and traps will be reduced. Thus, by depositing an oxide on the deposited layer, it is anticipated that there will be little dopant redistribution and a reduction of bulk charge and traps. Electrical characteristics will be determined. C-V and I-V measurements will be made to determine defects, such as trapped charge and interface charge. A primary goal of these experiments is to greatly increase the electrical characteristics of MOS structures in SiC. Ideally, electrical characteristics close to those of Si should be obtained, namely, a breakdown voltage of $\sim 1\times10^{7}$ V/cm, trap densities $\sim 10^{11}$–10^{10} cm^{-2} and interface state densities of $\sim 10^{10}$ cm^{-2}.

C. Conclusions

Current cleaning and surface preparation techniques for silicon may be inadequate in their current form for SiC. A residual oxide remains after the currently accepted cleaning techniques which may or may not affect the electrical characteristics of deposited oxides. The integrated UHV system will be able to explore processes that have previously been unobtainable. The uniqueness of the surface preparation integrated with the growth and characterization system allows for capabilities that have not been previously used in the characterization and growth of oxides on SiC. The electrical characteristics will guide the selection of the optimal process and the surface diagnostics should allow a scientific understanding of the process.

D. Future Research Plans and Goals

Establishing a base line procedure that is equivalent to the accepted procedure for oxide growth will enable considerable focus on the examination of the oxide layers for use as gate insulators in field effect devices. Once the base line procedure is established, a systematic

approach to surface preparation, initial insulator growth and insulator deposition will be implemented to determine a procedure that yields high-quality insulator on p-type SiC

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VII. P-type 4H and 6H-SiC High Voltage Schottky Barrier Diodes

A. Introduction

Silicon carbide has received increasing attention for power switching, microwave and high temperature application due to its high breakdown electric field, thermal conductivity and electron saturation drift velocity [1-3]. Although there have been many publications on high voltage Schottky contacts on n-type SiC, there is no work reported on high voltage (>100 V) Schottky contacts to p-type SiC. Lundberg *et al.* [4] reported cobalt Schottky contacts on n- and p-type 6H-SiC. However the purpose of the paper was to study the temperature stability of the contacts. Very little reverse breakdown data was reported on these diodes with maximum reverse bias applied on these diodes being limited to 5 V. Lundberg *et al.* [5] also reported tungsten Schottky contact to n- and p-type 6H-SiC. However, breakdown characteristics in these diodes were studied only up to a reverse bias of 100 V and no mention was made about the breakdown voltages of these diodes. Frojdh *et al.* [6] reported Schottky barrier diodes fabricated by evaporation of Ti on p-type 6H-SiC but the reverse characteristics were studied only up to a bias of -70 V. In these papers, no explanations were offered for the high forward voltage drops observed in these Schottky contacts on p-type SiC as compared to contacts on n-type 6H-SiC. In contrast with 6H-SiC, to our knowledge no work has been reported on Schottky contacts to p-type 4H-SiC. In this paper, we report for the first time the characteristics of Schottky contacts on both p-type 4H- and 6H-SiC with breakdown voltages as high as 600 V. Analysis of the series resistance observed in these diodes is also provided.

B. Experimental Results

The materials [7] used for the fabrication of the Schottky barrier diodes were aluminum doped 6H-SiC (5×10^{15} cm^{-3}, 1.6 μm thick) and 4H-SiC (1×1^{16} cm^{-3}, 2 μm thick) homo-epitaxial layers grown on off-axis 6H-SiC P^+ substrates (3×10^{18} cm^{-3}). Prior to the metal deposition, the SiC wafers were given a Huang clean (10 min dip in $NH_4OH:H_2O_2:H_2O$::1:1:5 followed by a ten minute dip in $HCl:H_2O_2:H_2O$::1:1:5 solution at 70°C). Schottky diodes (230 μm diameter) were fabricated using a shadow mask with sequential evaporation of Ti (1000 A) and Al (1000 A) layers. Blanket evaporation of a Ti/Al layer was also done on the heavily doped substrate to form a large area backside contact. The epitaxial doping concentration and thickness was determined using reverse biased capacitance-voltage (C-V) measurements. rom the C-V measurements, the average doping concentration in the drift region was determined to be $(6\pm1)\times10^{15}$ cm^{-3} for 6H-SiC and $(1\pm0.5)\times10^{16}$ cm^{-3} for 4H-SiC. The thickness of the epitaxial layer was found to be 1.6 μm for 6H-SiC and 2 μm for 4H-SiC. The

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Schottky barrier height was calculated to be 1.95 eV for 6H-SiC and 1.5 eV for 4H-SiC which is slightly higher than the value of the barrier height determined from the forward I-V measurements.

The measured forward current-voltage (I-V) characteristics of typical 6H-SiC and 4H-SiC Schottky rectifiers are shown in Fig. 1. Under forward biased conditions, the current conduction mechanism follows the thermionic emission theory at low current levels. However, at higher current density levels, a large series resistance is observed that contributes to an additional voltage drop across the diode. Thus, the forward voltage drop of the Schottky rectifier is given by:

$$V_F = \frac{\eta kT}{q} \ln\left(\frac{J_F}{A^* T^2}\right) + \eta\phi_{bn} + R_{s,sp} J_F, \qquad (1)$$

where k is the Boltzmann's constant, η is the ideality factor, T is the temperature, q is the electron charge, J_F is the current density, A^* is the effective Richardson's constant, $R_{s,sp}$ is the specific series resistance, and Φ_{bn} is the barrier height [8]. The ideality factor (η) was found to be 1.9 for 6H-SiC and 2.2 for 4H-SiC. The barrier height calculated from the forward I-V measurements was also found to be constant with temperature in the range 300–473 K, and had a value of 1.8 eV for 6H-SiC and 1.4 eV for 4H-SiC.

The forward voltage drop (V_F) for 4H-SiC was found to be 6 V and that for 6H-SiC was 13 V at 100 A/cm^2 (Current=3.14×10^{-4} A). The high forward drop in these p-type SiC Schottky diodes can be attributed to the large series resistance ($R_{s,sp}$) of the epitaxial drift layer and the substrate which arises as a result of the large ionization energy of the dopant atom (Al) in SiC. For the same doping concentration, the specific resistance for 6H-SiC is larger than that for 4H-SiC because the ionization energy for Al is 239 eV in 6H-SiC versus 191 eV in 4H-SiC [9]. The $R_{s,sp}$ values calculated from a plot of IdV/dI vs I was found to be 70 mΩ cm^2 in 6H-SiC and 25 mΩ cm^2 in 4H-SiC at room temperature. The $R_{s,sp}$ was found to monotonically decrease with temperature for both 4H- and 6H-SiC as shown in Fig. 2. After taking incomplete ionization into account [10], the carrier densities in the epilayer and the substrate in 6H-SiC were calculated to be 1.2×10^{15} cm^{-3} and 3×10^{16} cm^{-3}, respectively. Using a mobility value of 90 cm^2/Vsec in the epilayer and a value of 70 cm^2/Vsec in the substrate in 6H-SiC [11], the $R_{s,sp}$ in the epilayer and substrate were calculated to be 7 mΩ cm^2 and 70 mΩ cm^2, respectively. Similar calculations for 4H-SiC gave a $R_{s,sp}$ of 2.5 mΩ cm^2 in the epilayer by using a mobility of 115 cm^2/Vsec [11] and a carrier concentration of 5×10^{15} cm^{-3} and a $R_{s,sp}$ of 24 mΩ cm^2 in the substrate by using a mobility of 80 cm^2/Vsec [11] and a carrier concentration of 3×10^{16} cm^{-3}. The calculated total series resistances of 77 mΩ cm^2 for 6H-SiC and 26.5 mΩ cm^2 for 4H-SiC are in reasonable agreement with the measured values.

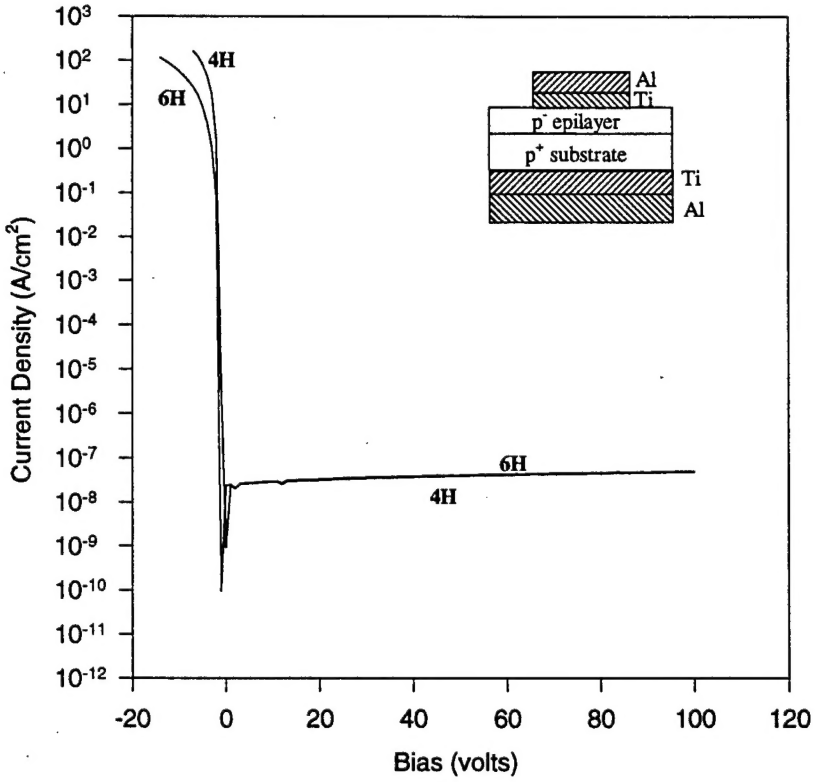

Fig. 1. I-V characteristics of a typical p-type 6H and 4H-SiC titanium Schottky diode.

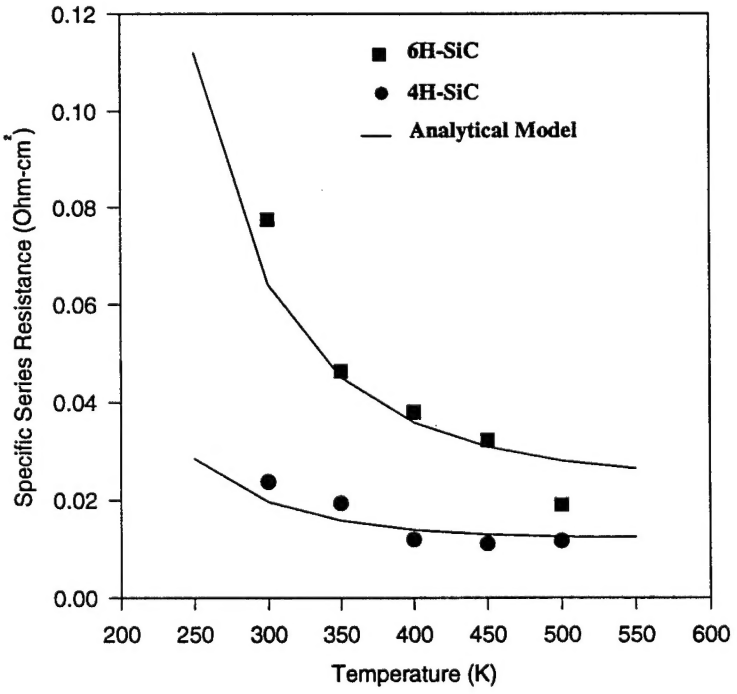

Figure 2. Variation of specific-on-resistance with temperature in 6H and 4H-SiC.

Thus, our calculations indicate that there is a substantial voltage drop in the substrate (~ 90%) caused by incomplete ionization of the carriers. With increasing temperature, the mobility decreases while the concentration of carriers increases. Assuming that the mobility varies as T^{-2} [12] for both 4H- and 6H-SiC the calculated $R_{s,sp}$ was found to decrease with temperature as shown by the solid curves in Fig. 2, which fits well with the experimental data.

The reverse I-V characteristics of the 6H- and 4H-SiC Schottky diodes were measured at temperatures ranging from 300–500 K. At room temperature, the reverse leakage current density in 4H- and 6H-SiC was extremely low (< 1×10^{-7} A/cm^2). At room temperature, 6H-SiC diodes exhibited a sharp breakdown at 540 V while the 4H-SiC Schottky diodes exhibited a breakdown voltage as high as 600 V. Breakdown voltages of 6H-SiC Schottky diodes were found to decrease from over 500 V at room temperature to 350 V at 500 K. This can be attributed to the negative temperature co-efficient of the breakdown electric field reported for SiC [3]. However, the breakdown voltages remained fairly constant, independent of temperature for the 4H-SiC Schottky diodes. The critical electric field for breakdown (E_C) was calculated using the measured breakdown data. Due to the small epilayer thickness, the breakdown voltage must be analyzed using punch-through breakdown conditions [8]. E_C values calculated for room temperature breakdown (assuming that breakdown is not limited by electric field crowding at the edges of the diodes) were 3.3×10^6 V/cm for p-type 6H-SiC and 2.9×10^6 V/cm for p-type 4H-SiC. These values are in good agreement with values reported for n-type 4H- and 6H-SiC [3] indicating that edge field crowding does not limit the breakdown voltage of the Schottky diode made on p-type SiC.

C. Conclusions

In conclusion, high voltage Schottky barrier diodes have been successfully fabricated by depositing titanium through a shadow mask on homoepitaxial p-type 6H and 4H-SiC layers. The barrier heights were estimated to be 1.8–2.0 eV for 6H-SiC and 1.4–1.5 eV for 4H-SiC at room temperature using both I-V and C-V measurements. The Schottky barrier diodes showed excellent reverse IV characteristic with leakage current density lower that 1×10^{-7} A/cm^2 at room temperature at a reverse bias of 100 V. The specific series resistances for 6H- and 4H-SiC was calculated to be 70 mΩ cm^2 and 25 mΩ cm^2, respectively. The series resistance was found to decrease with temperature because of an increase in the acceptor ionization in the epilayer and substrate for both 4H- and 6H-SiC. Critical electric field strength for breakdown was found to be 3.3×10^6 V/cm for 6H-SiC and 2.9×10^6 V/cm for 4H-SiC at a doping concentration of $(0.5–1)\times10^{16}$ cm^{-3}.

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